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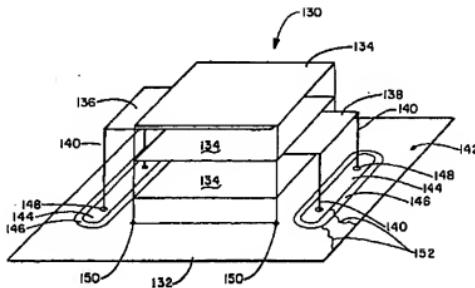
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(71) Applicant (for all designated States except US): XY ATTEN- UATORS, L.L.C. [US/US]; 2700 West 21st Street, Erie, PA 16506 (US).		Published With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.
(74) Agents: GAUM, R., Eric et al.; Oldham & Oldham Co., L.P.A., Twin Oaks Estate, 1225 West Market Street, Akron, OH 44313-7188 (US).		

(54) Title: ENERGY CONDITIONING CIRCUIT ASSEMBLY



(57) Abstract

The present invention is a component carrier (132) consisting of a plate of insulating material having a plurality of apertures (140) for accepting the leads of a thru-hole differential and common mode filter (130). Another embodiment consists of a surface mount component carrier (10) comprising a disk (15) of insulating material having a plurality of apertures (24). The same concept for the above described carrier is also incorporated into several alternate embodiments, either independently, embedded within electronic connectors. The overall configuration and electrical characteristics of the concepts underlying the present inventions are also described as an energy conditioning circuit assembly which encompasses the combination of differential and common mode filters and component carriers optimized for such filters. The various embodiments of components carriers provide increased physical support and protection to differential and common mode filters and substantially improve the electrical characteristics of the filter due to the increased shielding provided by the carriers. Embodiments of the carrier energy conditioning assembly include integrated circuit construction for a differential and common mode filter coupled to the power bus of an integrated circuit.

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1 ENERGY CONDITIONING CIRCUIT ASSEMBLY

2 Technical Field

3 This application is a continuation-in-part of copending U.S. Patent Application,
4 Serial No. 09/286,812 filed April 6, 1999, which is a continuation-in-part of U.S. Patent
5 Application, Serial No. 09/056,436 filed April 7, 1998. This application also claims the
6 benefit of U.S. Provisional Application No. 60/131,386 filed April 28, 1999, U.S.
7 Provisional Application No. 60/135,542 filed May 24, 1999, U.S. Provisional Application
8 No. 60/136,451 filed May 28, 1999, U.S. Provisional Application No. 60/139,182 filed
9 June 15, 1999, U.S. Provisional Application No. 60/146,987 filed August 3, 1999, U.S.
10 Provisional Application No. 60/165,035 filed November 12, 1999, U.S. Provisional
11 Application No. 60/180,101 filed February 3, 2000, and U.S. Provisional Application No.
12 60/185,320 filed February 28, 2000.

13 The invention includes the use of energy conditioning assemblies, pathway
14 intersections and layered architectures such as those described and claimed in
15 commonly owned U.S. Patent No. 5,909,350, U.S. Patent No. 6,018,448, and currently
16 pending U.S. Patent Application, Serial No. 09/008,769, all incorporated herein by
17 reference. A series of preferred embodiments are directed to energy conditioning that
18 occurs when unenergized elements are combined and electrified to act as part of a
19 circuit that provides conditioned energy to an integrated circuit or any other active
20 energy loads within electronic equipment or systems. The present invention also
21 provides electrical interference suppression and/or shielding for improved performance
22 of active electronic components located within larger electronic systems.

23 Background of the Invention

24 The majority of electronic equipment produced presently, and in particular
25 computers, communication systems, military surveillance equipment, stereo and home

1 entertainment equipment, televisions and other appliances include miniaturized
2 components to perform new high speed functions and electrical interconnections which
3 according to the materials from which they are made or their mere size are very
4 susceptible to stray electrical energy created by electromagnetic interference or voltage
5 transients occurring on electrical lines. Voltage transients can severely damage or
6 destroy such micro-electronic components or contacts thereby rendering the electronic
7 equipment inoperative, and requiring extensive repair and/or replacement at great cost.
8 Based upon the foregoing there was found a need to provide a multi-functioning
9 electronic component architecture which attenuates electromagnetic emissions resulting
10 from differential and common mode currents flowing within electronic circuits, single
11 lines, pairs of lines and multiple twisted pairs. Such multi-functioning electronic
12 components are the subject of commonly owned U.S. Patent No. 5,909,350 (application
13 Serial No. 08/841,940), continuation-in-part application Serial No. 09/008,769, and U.S.
14 Patent No. 6,018,448 (continuation-in-part application Serial No. 09/056,379), all
15 incorporated herein by reference.

16 While the above referenced electronic components accomplish their respective
17 tasks, usage of such components has been limited for a number of reasons. First, the
18 number of such components required continues to increase as applications, such as
19 data buses, continue to grow. In addition, as the number of required components
20 grows, so does the physical size of multi-component packages. Second, by their nature
21 the electronic components referred to are delicate structures which do not handle
22 physical stress well. During the manufacture of electronic products a number of
23 mechanical stresses associated with handling and soldering can damage the
24 components.

25 Another drawback to using the referenced electronic components is that it

1 becomes very tedious to manually handle and mount the components on electronic
2 products being assembled. This often time translates into lower product yields and
3 added expense due to broken or misconnected components. A further disadvantage
4 to some of the components is that they include leads for thru-hole insertion. Physical
5 stressing, bending or applying torque to the leads can cause a failure in the final
6 product, either immediately or later thereby affecting the products overall reliability.

7 Another source of electrical noise found in prior art differential mode filters,
8 common mode filters and capacitor decouplers is caused by imperfections in the
9 capacitors that make up the filters and decouplers. The effects of these imperfections
10 are commonly referred to as parasitic effects. Parasitic or non-ideal capacitor behavior
11 manifests itself in the form of resistive and inductive elements, nonlinearity and
12 dielectric memory. The four most common effects are leakage or parallel resistance,
13 equivalent series resistance (ESR), equivalent series inductance (ESL) and dielectric
14 absorption. The equivalent series resistance (ESR) of a capacitor is the resistance of
15 the capacitor leads in series with the equivalent resistance of the capacitor plates. ESR
16 causes the capacitor to dissipate power during high flowing ac currents. The equivalent
17 series inductance (ESL) of a capacitor is the inductance of the capacitor leads in series
18 with the equivalent inductance of the capacitor plates. An additional form of parasitic
19 that goes beyond the component itself is stray capacitance which is attributed to the
20 attachment of the capacitor element within an electrical circuit. Stray capacitors are
21 formed when two conductors are in close proximity to each other and are not shorted
22 together or screened by a Faraday shield. Stray capacitance usually occurs between
23 parallel traces on a PC board or between traces/planes on opposite sides of a PC
24 board. Stray capacitance can cause problems such as increased noise and decreased

1 frequency response.

2 Several other sources of electrical noise include cross talk and ground bounce.
3 Cross talk in most connectors or carriers is usually the result of mutual inductance
4 between two adjacent lines rather than from parasitic capacitance and occurs when
5 signal currents follow the path of least inductance, especially at high frequencies, and
6 return or couple onto nearby conductors such as conductive tracks positioned parallel
7 with or underneath the signal current track. Ground bounce is caused by shifts in the
8 internal ground reference voltage due to output switching of a component. Ground
9 bounce causes false signals in logic inputs when a device output switches from one
10 state to another. It has been found that the multi-functioning electronic components,
11 specifically the differential and common mode filters and decouplers disclosed in the
12 above referenced, commonly owned U.S. patent applications, provide improved
13 performance when coupled or used with an enlarged ground shield that can
14 substantially decrease or reduce and in some cases can eliminate capacitor parasitics,
15 stray capacitance, mutual inductive coupling between two opposing conductors, various
16 forms of cross talk and ground bounce.

17 Therefore, in light of the foregoing deficiencies in the prior art, the applicant's
18 invention is herein presented.

19 Summary of the Invention

20 Based upon the foregoing, there has been found a need to provide a component
21 carrier which is less susceptible to mechanical stresses and shock, more easily
22 assembled, surface mountable and capable of being used in automated assembly.

23 It is therefore a main object of the present invention to provide a component
24 carrier for maintaining one or more surface mount components.

1 It is another object of the present invention to provide a component carrier which
2 is less susceptible to mechanical stresses imparted upon components during various
3 manufacturing processes.

4 It is also an object of the present invention to provide a component carrier having
5 an enhanced ground surface which improves the functional characteristics of surface
6 mount components coupled to the component carrier.

7 It is a further object of the present invention to provide a component carrier
8 adapted specifically to receive a differential and common mode filter and decoupler as
9 disclosed in the above referenced, commonly owned pending U.S. patent applications.

10 It is a further object of the present invention to provide a component carrier
11 having an enhanced ground surface which improves the functional characteristics of
12 differential and common mode filters and decouplers as disclosed in the above
13 referenced, commonly owned pending U.S. patent applications.

14 It is a further object of the present invention to provide an energy conditioning
15 circuit assembly that combines a component carrier with a differential and common
16 mode filter and decoupler as disclosed in the above referenced, commonly owned
17 pending U.S. patent applications to thereby provide simultaneous filtering of common
18 and differential mode interference, suppression of parasitic or stray capacitance,
19 mutual inductive coupling between two adjacent conductors and circuit decoupling from
20 a single assembly.

21 It is another object of the present invention to provide an integrated circuit
22 construction for a differential and common mode filter coupled to the power bus lines
23 servicing the integrated circuit.

24 These and other objects and advantages of the present invention are

1 accomplished through the use of various embodiments of a component carrier which
2 receives either a thru-hole or surface mount differential and common mode filter and
3 decoupler as disclosed in the above referenced, commonly owned U.S. patents and
4 pending U.S. patent applications (hereinafter referred to as "differential and common
5 mode filter" or "layered architecture").

6 One embodiment consists of a plate of insulating material, also referred to as a
7 planar insulator, having a plurality of apertures for accepting the leads of a thru-hole
8 differential and common mode filter. Another embodiment consists of a surface mount
9 component carrier comprised of a disk of insulating material having at least two
10 apertures. The disk is substantially covered by a metalized or conductive ground
11 surface and includes at least two conductive pads surrounding the apertures, and
12 insulating bands which surround each conductive pad. The insulating bands separate
13 and electrically isolate the conductive pads from the metalized ground surface. A
14 surface mount component, such as a differential and common mode filter, is positioned
15 lengthwise between the two conductive pads and operably coupled to the carrier. Once
16 the surface mount component is coupled to the carrier, the combination can be
17 manipulated, either manually or through various types of automated equipment, without
18 subjecting the surface mount component to mechanical and physical stresses normally
19 associated with the handling of miniature components. The carrier also provides the
20 added benefit of improved shielding from electromagnetic interference and over voltage
21 dissipation due to the surface area of the metalized ground surface.

22 The same concept for the above described carrier is also incorporated into
23 several alternate embodiments, either independently, embedded within electronic
24 connectors or configured for use with electric motors. The overall configuration and

1 electrical characteristics of the concepts underlying the present inventions are also
2 described as a conditioning assembly (also referred to as an energy conditioning circuit
3 assembly or "ECCA") which encompasses the combination of differential and common
4 mode filters and component carriers optimized for such filters.

5 These along with other objects and advantages of the present invention will
6 become more readily apparent from a reading of the detailed description taken in
7 conjunction with the drawings and the claims.

8 Brief Description of the Drawings

9 Fig. 1A is a perspective, exploded view of a thru-hole differential and common
10 mode filter coupled to a portion of the thru-hole component carrier of the present
11 invention;

12 Fig. 1B is a perspective, exploded view of a differential and common mode filter
13 coupled to a portion of a carrier circuit;

14 Fig. 2 is an elevational view in cross section of a single-sided surface mount
15 component carrier of the present invention;

16 Fig. 3 is a top plan view of the surface mount component carrier shown in Fig.
17 2;

18 Fig. 4 is an elevational view in cross section of a double-sided surface mount
19 component carrier of the present invention;

20 Fig. 5 is a top plan view of the surface mount component carrier shown in Fig.
21 4;

22 Fig. 6 is an elevational view in cross section of an alternate embodiment of a
23 single-sided surface mount component carrier of the present invention;

24 Fig. 7 is a top plan view of the surface mount component carrier shown in Fig.

1 6;

2 Fig. 8 is an elevational view in cross section of an alternate embodiment of a
3 double-sided surface mount component carrier of the present invention;

4 Fig. 9 is a top plan view of the surface mount component carrier shown in Fig.

5 8;

6 Fig. 10 is a partial perspective view of a further embodiment of a connector
7 surface mount differential and common mode filter carrier of the present invention;

8 Fig. 11 is a partial top plan view of the connector surface mount differential and
9 common mode carrier shown in Fig. 10;

10 Fig. 12A is a top plan view of a carrier energy conditioning circuit assembly of
11 the present invention; and Fig. 12B is a side elevational view of the carrier energy
12 conditioning circuit assembly shown in Fig. 12A; Fig. 13A is a top plan view of a carrier
13 energy conditioning circuit assembly applied to a crystal base portion of a crystal
14 component; Fig. 13B is a side elevational view of the carrier energy conditioning circuit
15 assembly applied to a crystal base portion of a crystal component shown in Fig. 13A;
16 Fig. 13C is a front elevational view of the carrier energy conditioning circuit assembly
17 enclosed in a crystal component application shown in Fig 13B with a metal enclosure;
18 and Fig. 13D is a side elevational view of the carrier energy conditioning circuit
19 assembly enclosed in a crystal component application shown in Fig. 13C;

20 Fig. 14A is a top plan view of a carrier energy conditioning circuit assembly
21 comprising a differential and common mode filter mounted on a single layer substrate
22 carrier within an integrated circuit package; and Fig. 14B is a top plan view of a single
23 point ground area located beneath the differential and common mode filter in Fig. 14A;

24 Fig. 15 is a top plan view of a carrier energy conditioning circuit assembly

1 comprising a differential and common mode filter mounted transversely on a single
2 layer substrate carrier within an integrated circuit package;

3 Fig. 16A is a top plan view of a two layer substrate carrier having a differential
4 and common mode filter mounted to bus traces on a top surface of the carrier; and Fig.
5 16B is a front cross-sectional view of the two layer substrate carrier of Fig. 16A; and
6 Fig. 16C is a side sectional view of the two layer substrate carrier of Fig. 16A; and Fig
7 16D is a front cross-sectional view of an alternate embodiment of the two layer
8 substrate carrier of Fig. 16A which includes an insulation layer;

9 Fig. 17A is a top plan view of a three layer substrate carrier having a differential
10 and common mode filter mounted to power bus traces on a top surface of the carrier;
11 and Fig. 17B is a front cross-sectional view of the three layer substrate carrier of Fig.
12 17A; and Fig. 17C is a side sectional view of the three layer substrate carrier of Fig.
13 17A; and Fig. 17D is a front cross-sectional view of the three layer substrate carrier of
14 Fig. 17A including a top potting layer;

15 Fig. 18 is a side sectional view of a multi-layer substrate carrier having a
16 differential and common mode filter embedded on a layer within the substrate;

17 Fig. 19A is a top plan view of a shielded twisted pair feed through differential and
18 common mode filter; and Fig. 19B is a top plan view of the coplanar elements that
19 comprise the shielded twisted pair feed through differential and common mode filter of
20 Fig. 19A; and Fig. 19C and Fig. 19D are schematic representations of a shielded
21 twisted pair feed through differential and common mode filter showing differential noise
22 cancellation; and Fig. 19E and Fig. 19F are schematic representations of a shielded
23 twisted pair feed through differential and common mode filter showing common mode
24 noise cancellation;

1 Fig. 20A is a top plan view of a carrier energy conditioning circuit assembly
2 comprising a shielded twisted pair feed through differential and common mode filter
3 embedded in a multi-layer substrate carrier within an integrated circuit package; and
4 Fig. 20B is a front cross-sectional view of the integrated circuit package of Fig. 20A; and
5 Fig 20C is a top plan view of the ground plane layer of the integrated circuit package
6 of Fig. 20A;

7 Fig. 21 is a top plan view of a carrier energy conditioning circuit assembly
8 comprising a shielded twisted pair feed through differential and common mode filter
9 mounted underneath a multi-layer substrate carrier within an integrated circuit package;
10 and

11 Detailed Description of the Preferred Embodiments

12 Fig. 1A shows the present invention in its simplest form. Component carrier 132
13 is shown coupled with a differential and common mode filter 130 having thru-hole leads
14 140 for electrical coupling to carrier 132. Differential and common mode filter 130 is
15 disclosed in commonly owned U.S. Patent No. 5,909,350 (Serial No. 08/841,940);
16 application Serial No. 09/008,769; and U.S. Patent No. 6,018,448 (Serial No.
17 09/056,379), incorporated herein by reference. Briefly, the structure of differential and
18 common mode filter 130 will be described. Filter 130 consists of a first electrode 136
19 and a second electrode 138 which are physically separated by and electrically isolated
20 from each other by a plurality of ground layers 134 and by a dielectric medium. The
21 particular architecture creates a line-to-line capacitor and two line-to-ground capacitors
22 which provide for differential and common mode filtering and decoupling.

23 Because filter 130 is a somewhat fragile component, component carrier 132
24 provides a physical support to which filter 130 is physically and electrically coupled.

1 The first and second electrodes 136 and 138 each have one or more conductive leads
2 140 which are inserted into apertures 148 of conductive pads 144. Each conductive
3 pad 144 is electrically isolated from the conductive surface 142 of component carrier
4 132 by insulating bands 146. Not only does component carrier 132 provide additional
5 physical strength to differential and common mode filter 130 but it also acts as a
6 conductive shield, which substantially improves the electrical characteristics of filter 130.
7 When filter 130 is properly coupled to carrier 132 the plurality of common conductive
8 electrodes or layers 134 are electrically coupled to one another and then electrically
9 coupled to conductive surface 142 by any number of means known by those of ordinary
10 skill in the art. One common means of coupling is through the use of solder points 150
11 connecting portions of the common conductive layers 134 to conductive surface 142.
12 One advantage to the relatively large conductive surface 142 of component carrier 132
13 is that if cracks 152 appear or form on conductive surface 142 its shielding effect is not
14 lost.

15 Fig. 1B shows an alternate version of the present invention in its simplest form.
16 The difference in Fig. 1B as compared to Fig. 1A is that the carrier 132' of Fig. 1B has
17 a pair of circuit traces 145A insulated from conductive surface 142A by insulating bands
18 146A. A person of ordinary skill in the art would understand that the combination is not
19 limited by a specific number of circuit traces that can be coupled to the respective
20 conductors 140A. First electrode 136 and second electrode 138 are each electrically
21 connected through conductor 140A to a solder pad 144A on one of the circuit traces
22 145A and coupled thereto by solder 150A. Common conductive layers 134 are
23 electrically connected by conductor 140A to conductive surface 142A. It should be
24 noted that each embodiment can include one or more connections between the

1 common conductive layers 134 and conductive surface 142A. In one preferred
2 embodiment, there are at least two conductors 140A that electrically connect the
3 common conductive layers 134 to the conductive surface 142A.

4 Both embodiments shown in Figs. 1A and 1B disclose a layered architecture
5 (differential and common mode filter 130) in combination with a conductive substrate
6 (carrier 132) that comprises an energy conditioning circuit assembly (hereinafter
7 "ECCA"). When the ECCA is coupled between an energy source and an active
8 load, the ECCA receives and conditions energy propagating to the load in a
9 balanced manner. The ECCA of the present invention is disclosed in a plurality of
10 embodiments, which will be described subsequently. Each embodiment of the
11 ECCA receives and conditions energy when electrically coupled between an active
12 load and an energy source. The conditioning functions provided by the ECCA are
13 facilitated, in part, by the physical and electrical connection of the common
14 conductive electrodes (ground layers 134) of the layered architecture with an
15 external conductive path provided by the conductive substrate. The conductive
16 substrate is positioned apart from the differentially energized electrodes of the
17 layered architecture. The common conductive electrodes alone or in combination
18 with the conductive substrate are normally electrically coupled to a separate energy
19 path from the energy path between first electrode or layer 136 and conductive area
20 142 (or 142A) and second electrode or layer 138 and conductive area 142 (or
21 142A), at the same time. Depending upon the intended application of the ECCA, the
22 common conductive electrodes and/or the conductive substrate may be connected
23 to a circuit ground or return, an isolated ground, a chassis ground, or earth ground.
24 As a person of ordinary skill in the art would understand, the energy return path

1 could be any desired reference including a zero voltage reference or even a offset
2 reference in either the positive or negative direction, as used for inverted digital logic
3 for example. For simplicity, the term ground will be used generally but is not
4 intended to be limited to any one particular electrical reference point.

5 When one or more pairs of differential electrodes (first and second electrodes
6 136 and 138 respectively) of the layered architecture are electrically connected to
7 external energy pathways or planes, i.e., electrical connections to and from a power
8 source and load, and energy is applied to the pathways, the ECCA performs
9 simultaneous energy conditioning functions. These conditioning functions include
10 but are not limited to filtering of common mode and differential mode noise,
11 bypassing of noise to ground, circuit decoupling and/or transient voltage
12 suppression or minimization. Depending upon the type of energy source and load,
13 the ECCA may also perform primarily an energy conditioning function or simply a
14 circuit decoupling function, however in many applications it will perform multiple
15 functions as just described upon propagating energy, simultaneously.

16 The ECCA can act as a system conduit for energy propagating along multiple
17 external energy pathways. Energy will also propagate within the layered
18 architecture in a balanced manner from multiple directions 3 dimensionally; meaning
19 the reactance of the propagated energy will be approximately balanced. Due to the
20 unique arrangement of the ECCA, energy received and conditioned provides an
21 active load with a defacto constant energy source, which can be drawn upon by the
22 active load without detrimental voltage drops.

23 The ECCA also effectively minimizes loop currents or unwanted emissions
24 that would otherwise exist in the form of common mode noise coupled to energy

1 pathways or conductive planes. The ECCA also prevents radiation of common
2 mode noise that would detrimentally influence the energy coupled to the loads
3 serviced by the ECCA. Because the common conductive electrodes of the layered
4 architecture are electrically connected to the larger conductive area of the
5 conductive substrate, the larger conductive area becomes an extension of the
6 common conductive electrodes found within the layered architecture, and
7 conversely, common conductive electrodes found within the layered architecture
8 become an extension of the larger conductive area of the conductive substrate.

9 When the differential pathways are coupled to an active load, for example the
10 silicon wafer or active integrated circuit, the conductive substrate extension is in a
11 position such that it nearly comes in contact with the differential conductive pathways
12 containing energy that is propagating to and from a source and a load. This parallel
13 positioning technique of propagating energy paths minimizes the distance of separation
14 or loop area between energy propagating along a source pathway to a load and the
15 loop area of the pathway used by energy as it returns back to its source. This
16 technique helps to minimize any RF energy that could develop and radiate as common
17 mode noise originating from the layered architecture arrangement back into the
18 circuitry. The common conductive layers also provide a physical barrier of separation
19 interposed between differential conductive electrodes and at the same time, in an
20 energized state, it also acts as a common electrostatic shield that functions between
21 a dielectric medium to partially enveloping the differential conductors contained
22 internally within the layered architecture of the ECCA.

23 The larger conductive area or extension provided to the common conductive
24 electrodes within the layered architecture functions as an enveloping shield that

1 decreases unwanted energy radiating from the differential electrodes that would
2 otherwise detrimentally affect nearby energy propagating along the differentially
3 phased opposite conductors. The energized combination that makes up the ECCA
4 provides efficient simultaneous conditioning and/or decoupling on portions of energy
5 propagating across the internal energy pathways or planes that are servicing a load.

6 The parallel arrangement of the common conductive electrodes within the
7 layered architecture and the extension into the same of the externally located
8 conductive area provided by the conductive substrate also functions to minimize
9 and/or suppress unwanted parasitics and emissions. Such emissions can radiate
10 from or be received by portions of internal differential energy pathways as energy
11 propagates along the internal energy pathways to an active load. Portions of the
12 energy radiated from the internal energy pathways that is trapped within the
13 boundary formed by the layered architecture and the larger conductive area of the
14 conductive substrate will be returned to its source. The opposing differentially
15 phased conductors within the layered architecture will also suppress or minimize
16 electromagnetic emissions of portions of the propagating energy not contained
17 electrostatically by the common conductive pathways by utilizing the commonly known
18 principals of inductive cancellation between closely positioned yet opposing, energy
19 pathways. Some or all of any undesirable energy (signals, noise, and/or transients)
20 conditioned and/or decoupled by the ECCA will be contained, suppressed and/or
21 bypassed to the common conductive electrodes of the layered architecture and the
22 larger conductive area provided by the conductive substrate. The foregoing
23 functional description of the ECCA applies generally to all of the embodiments of the
24 invention set forth hereinafter. Each subsequently described alternative

1 embodiment is to be interpreted in light of the foregoing descriptions.

2 A more specific embodiment of the present invention illustrated in Fig. 2 is

3 surface mount component carrier 10 for maintaining a ceramic planar surface mount

4 electrical component, such as a differential and common mode filter as is disclosed

5 in commonly owned U.S. Patent No. 5,909,350 (Serial No. 08/841,940); application

6 Serial No. 09/008,769; and U.S. Patent No. 6,018,448 (Serial No. 09/056,379),

7 incorporated herein by reference. Carrier 10 is a disk comprised of an insulator 14,

8 such as ceramic, having at least two apertures 18. Insulator 14 is covered by a

9 conductive metalized ground surface 16, at least two conductive pads 24

10 surrounding apertures 18, and insulating bands 22 surrounding each conductive pad

11 24. Throughout the written description "insulator" or "insulating material" may also

12 be referred to as "planar insulator." Insulating bands 22 separate and electrically

13 isolate conductive pads 24 from metalized ground surface 16. In the top plan view

14 of carrier 10, shown in Fig. 3, the preferred embodiment of the invention is circular in

15 shape with square insulating bands 22 surrounding partially rounded conductive

16 pads 24. Carrier 10 and its various elements can be formed into many different

17 shapes and Applicant does not intend to limit the scope of the invention to the

18 particular shapes shown in the drawings.

19 Referring again to Fig. 2, in the preferred embodiment, metalized ground surface

20 16 covers a substantial portion of the top and sides of carrier 10. Through-hole plating

21 20 covers the inner walls of aperture 18 and electrically couples to the corresponding

22 conductive pad 24. Through-hole plating 20 provides greater surface area for electrical

23 coupling of conductors 34 to conductive pads 24 as the conductors 34 are disposed

24 through apertures 18. The configuration of metalized ground surface 16, insulating

1 bands 22 and conductive pads 24 provide the necessary contacts for connecting a
2 surface mount component, such as differential and common mode filter 12, to the upper
3 surface of carrier 10, which in turn provides electrical connection between conductors
4 34 and surface mount component 12. The surface mount components referred to, such
5 as differential and common mode filter 12, are provided in standard surface mount
6 packages which include a number of solder terminations for electrically coupling the
7 device to external circuitry or in this case to carrier 10. Filter 12 includes first differential
8 electrode band 28 and second differential electrode band 30 extending from either end
9 of filter 12. Extending from the center of filter 12 is at least one and more typically two,
10 common ground conductive bands 26. An insulated outer casing 32 electrically isolates
11 first and second differential electrode bands 28 and 30 and common ground conductive
12 bands 26 from one another. A top plan view of a standard surface mount device as just
13 described is shown in Fig. 11 as differential and common mode filter 104. The filter 104
14 is comprised of first differential conductive band 116, second differential conductive
15 band 118 and two common ground conductive bands 120. The insulated outer casing
16 122 separates and electrically isolates each of the various conductive bands from one
17 another.

18 Fig. 1A shows the present invention in its simplest form. Component carrier 132
19 is shown coupled with a differential and common mode filter 130 having thru-hole leads
20 140 for electrical coupling to carrier 132. Differential and common mode filter 130 is
21 disclosed in commonly owned U.S. Patent No. 5,909,350 (Serial No. 08/841,940);
22 application Serial No. 09/008,769; and U.S. Patent No. 6,018,448 (Serial No.
23 09/056,379), incorporated herein by reference. Briefly, the structure of differential and
24 common mode filter 130 will be described. Filter 130 consists of a first electrode 136

1 and a second electrode 138 which are separated by and electrically isolated from a
2 plurality of ground layers 134 and each other by a dielectric medium. The particular
3 architecture creates a line-to-line capacitor and two line-to-ground capacitors which
4 provide for differential and common mode filtering and decoupling.

5 Because filter 130 is a somewhat fragile component, component carrier 132
6 provides a physical support to which filter 130 is electrically coupled. The first and
7 second electrodes 136 and 138 each have conductive leads 140 which are inserted into
8 apertures 148 of conductive pads 144. Each conductive pad 144 is electrically isolated
9 from the conductive surface 142 of component carrier 132 by insulating bands 146. Not
10 only does component carrier 132 provide additional physical strength to differential and
11 common mode filter 130 but it also acts as a ground shield which substantially improves
12 the electrical characteristics of filter 130. When filter 130 is properly coupled to carrier
13 132 the plurality of ground layers 134 are electrically coupled to one another and then
14 coupled to conductive surface 142 by any number of means known by those of ordinary
15 skill in the art. One common means of electrical coupling is through the use of solder
16 150 points connecting portions of the ground layers 134 to conductive surface 142.
17 One advantage to the relatively large conductive surface 142 of component carrier 132
18 is that if cracks 152 or electrical openings form on conductive surface 142 its shielding
19 effect is not lost.

20 Fig. 1B shows an alternate version of the present invention in its simplest form.
21 The difference in Fig. 1B as compared to Fig. 1A is that the carrier 132' of Fig. 1B has
22 a pair of circuit traces 145A insulated from conductive surface 142A by insulating bands
23 146A. First electrode 136 and second electrode 138 are each electrically connected
24 through conductor 140A to a solder pad 144A on one of the circuit traces 145A and

1 coupled thereto by solder 150A. Ground layers 134 are electrically connected through
2 conductor 140A to conductive surface 142A.

3 Both embodiments shown in Figs. 1A and 1B disclose a layered architecture
4 (differential and common mode filter 130) in combination with a conductive substrate
5 (carrier 132) that comprises an energy conditioning circuit assembly (hereinafter
6 "ECCA"). When the ECCA is coupled between an energy source and an active
7 load, the ECCA simultaneously receives and conditions energy propagating to the
8 load in a differentially balanced manner. The ECCA of the present invention is
9 disclosed in a plurality of embodiments, which will be described subsequently. Each
10 embodiment of the ECCA simultaneously receives and conditions energy when
11 coupled between an active load and an energy source. The conditioning functions
12 provided by the ECCA are facilitated, in part, by the electrical connection of the
13 common conductive electrodes (ground layers 134) of the layered architecture with
14 an external conductive path provided by the conductive substrate. The conductive
15 substrate is positioned apart from the differentially energized electrodes of the
16 layered architecture. The common conductive electrodes alone or in combination
17 with the conductive substrate are normally electrically coupled to an energy return
18 path, i.e., ground. Depending upon the intended application of the ECCA, the
19 common conductive electrodes and/or the conductive substrate may be connected
20 to a circuit ground or return, an isolated ground, a chassis ground, or earth ground.
21 As a person of ordinary skill in the art would understand, the energy return path
22 could be any desired reference including an offset reference in either the positive or
23 negative direction, as used for inverted digital logic for example. For simplicity, the
24 term ground will be used generally but is not intended to be limited to any one

1 particular electrical reference point.

2 When one or more pairs of differential electrodes (first and second electrodes
3 136 and 138 respectively) of the layered architecture are electrically connected to
4 external energy pathways or planes, i.e., electrical connections to and from a power
5 source and load, and energy is applied to the pathways the ECCA simultaneously
6 performs energy conditioning and decoupling. Depending upon the type of energy
7 source and load, the ECCA may perform only energy conditioning or decoupling,
8 although in many applications it will perform both upon propagating energy
9 simultaneously.

10 The ECCA can receive and source energy along multiple external energy
11 pathways. Energy will also propagate within the layered architecture in a balanced
12 manner, meaning the reactance of the propagated energy will be approximately
13 equal. Due to the unique arrangement of the ECCA, energy received and
14 conditioned provides an active load with a defacto constant energy source which
15 can be drawn upon by the active load.

16 The ECCA also effectively minimizes loop currents that would otherwise exist
17 in the energy pathways or planes coupled to the loads. Because the common
18 conductive electrodes of the layered architecture are electrically connected to the
19 larger conductive area of the conductive substrate, the larger conductive area
20 becomes an extension of the common conductive electrodes found within the
21 layered architecture. When coupled to an active load, for example the silicon wafer
22 of an integrated circuit, the conductive substrate will be positioned such that it nearly
23 comes in contact with the active load thereby minimizing the distance of separation
24 or loop area. This close positioning relationship of the active load, the conductive

1 substrate, and the layered architecture minimizes the current loop path of the
2 differentially energized electrodes, which are separated by dielectric medium. The
3 larger conductive area or extension provided to the common conductive electrodes
4 functions as an enveloping shield that decreases electrostatic energy. The
5 combination that makes up the ECCA provides efficient simultaneous conditioning
6 and/or decoupling of energy propagating across portions of the external energy
7 pathways or planes.

8 The parallel arrangement of the common conductive electrodes within the
9 layered architecture and the externally located conductive area provided by the
10 conductive substrate also functions to cancel and/or suppress unwanted parasitics
11 and electromagnetic emissions. Such emissions can radiate from or be received by
12 portions of external differential energy pathways as energy propagates along the
13 external energy pathways to an active load. Portions of the energy radiated from the
14 external energy pathways that is trapped within the boundary formed by the layered
15 architecture and the larger conductive area of the conductive substrate will be
16 returned to its source. Some or all of any undesirable energy (signals, noise, and/or
17 transients) conditioned and/or decoupled by the ECCA will be contained,
18 suppressed and/or bypassed to the common conductive electrodes of the layered
19 architecture and the larger conductive area provided by the conductive substrate.
20 The foregoing functional description of the ECCA applies generally to all of the
21 embodiments of the invention set forth hereinafter. Each subsequently described
22 alternative embodiment is to be interpreted in light of the foregoing descriptions.

23 Fig. 2 shows filter 12 positioned upon the top surface of carrier 10 so that the
24 common ground conductive bands 26 come in contact with the portion of the metallized

1 ground surface 16 which separates both of the insulating bands 22 from one another.
2 This is accomplished by positioning differential and common mode filter 12 lengthwise
3 between the two conductive pads 24 such that first differential electrode band 28 is in
4 contact with one of the two conductive pads 24 and second differential electrode band
5 30 comes in contact with the other conductive pad 24. Once filter 12 has been
6 positioned, by default, insulated outer casing 32 of filter 12 aligns with portions of
7 insulating bands 22 thereby maintaining electrical isolation between the various
8 conductive and electrode bands of filter 12. First and second differential conductive
9 bands 28 and 30 and the common ground conductive bands 26 consist of solder
10 terminations found in typical surface mount devices. Once filter 12 is positioned upon
11 carrier 10 standard solder reflow methods are employed causing the solder terminations
12 to reflow thereby electrically coupling and physically bonding filter 12 to carrier 10.
13 Customary solder reflow methods which can be used include infrared radiation (IR),
14 vapor phase and hot air ovens or any other means which can be used to expose the
15 solder to sufficiently elevated temperatures. Once differential and common mode
16 surface mount filter 12 is coupled to carrier 10, the combination of the two parts can be
17 manipulated, either manually or through various types of automated equipment, without
18 subjecting filter 12 to mechanical and physical stresses normally associated with the
19 handling of miniature and delicate electronic components.

20 Once coupled to carrier 10, filter 12 is electrically connected to external circuitry
21 through conductors 34 which may consist of wire leads or lengths of flexible wire. Once
22 disposed through apertures 18, conductors 34 are soldered to conductive pads 24 and
23 within apertures 18. Thru-hole plating 20 allows solder applied to conductive pads 24
24 and conductors 34 to flow into apertures 18 thereby adhering to the thru-hole plating.

1 Component carrier 10 reduces mechanical and physical stresses such as shock,
2 vibration and various thermal conditions which filter 12 would otherwise be subjected
3 to and provides a complete ground shield for filter 12. Because carrier 10 has a greater
4 surface area than filter 12 and a substantial portion of that surface area is covered by
5 metallized ground surface 16, carrier 10 acts as a ground shield which absorbs and
6 dissipates electromagnetic interference and over voltages. These added benefits
7 improve the overall functional performance and characteristics of filter 12.

8 Figs. 4 and 5 illustrate a further alternate embodiment of the present invention,
9 that being double-sided carrier 40. Carrier 40 is identical to carrier 10, as shown in Fig.
10 2, except that carrier 40 is double-sided and as a bottom surface which is substantially
11 identical to the top surface. This configuration allows two differential and common
12 mode surface mount filters 12a and 12b to be mounted to the upper and lower surfaces
13 of carrier 40. As illustrated in Fig. 4, metallized ground surface 16 covers substantial
14 portions of the top, sides and bottom of carrier 40 providing a greater overall surface
15 area. The increased surface area of metallized ground surface 16 imparts greater
16 shielding characteristics in carrier 40 which absorb and dissipate electromagnetic
17 interference. In addition, both the top and bottom of carrier 40 include corresponding
18 conductive pads 24 which are electrically connected to one another by thru-hole plating
19 which covers the inner walls of apertures 18.

20 Double-sided carrier 40 is also advantageous in that it allows for flexibility
21 needed to meet electromagnetic interference (EMI) and surge protection requirements
22 simultaneously through integration of different surface mount components on the same
23 carrier substrate. As an example, a differential and common mode filter, as previously
24 described, could be coupled to the top of carrier 40 while a MOV device could be

1 coupled on the bottom of carrier 40 effectively placing the filter and MOV devices in
2 parallel to provide EMI and surge protection in one compact, durable package.
3 Because carrier 40 provides a rigid base for maintaining various electronic surface
4 mount components, the components themselves are subjected to less physical stress
5 during manufacturing processes which in turn increases yields and lowers
6 manufacturing costs.

7 Fig. 5 shows a modified configuration of metallized ground surface 16,
8 conductive pads 24 and insulating bands 22. In this alternative embodiment, insulating
9 bands 22 have been substantially increased such that the surface area of carrier 40 is
10 substantially covered by insulation as opposed to a metallized ground surface. This
11 configuration can be used when decreased shield characteristics are desired or the
12 particular interaction between carrier 40 and the surface mount component needs to be
13 precisely controlled. One example is when parasitic capacitance values must be
14 maintained below a certain level. Note that the particular shapes of insulating bands
15 22, shown in Fig. 5, are not necessary. All that is required is that the surface area
16 covered by metallized ground surface 16 be varied which in turn varies the electrical
17 characteristics of double-sided carrier 40. It should also be noted that the surface
18 pattern shown in Fig. 3 can be used with the double-sided carrier 40, shown in Fig. 4,
19 or the surface pattern shown in Fig. 5 could just as easily be used with carrier 10,
20 shown in Fig. 2. To obtain further control the electrical characteristics of double-
21 sided carrier 40, one surface could be configured as shown in Fig. 5 while the other
22 surface, either top or bottom, could be configured as shown in Fig. 3. Altering the upper
23 and lower surface patterns of double-sided carrier 40 depending upon the types of
24 surface mount components coupled to carrier 40 allows for obtaining optimal electrical

1 characteristics as needed.

2 Figs. 6 through 9 illustrate further alternate embodiments of the single and
3 double-sided carriers shown in Figs. 2 through 5. Referring to Fig. 6, single-sided
4 carrier 50 is similar to carrier 10 of Fig. 2 except that carrier 50 includes a conductive
5 core 38 imbedded within insulator 14 which is electrically coupled to metalized ground
6 surface 16. As shown in Figs. 6 and 7, conductive core 38 abuts and comes in contact
7 with metalized ground surface 16 along the sides of carrier 50. A via 36 is disposed
8 within the center of carrier 50 which provides an additional electrical connection
9 between the metalized ground surface 16 which covers the top of carrier 50 and
10 conductive core 38. Via 36 is a small aperture formed in the surface of carrier 50 which
11 passes through insulator 14 and comes in contact with conductive core 38. Although
12 not shown, via 36 includes thru-hole plating which electrically connects conductive core
13 38 and metalized ground surface 16. Fig. 7 shows the surface configuration for carrier
14 50 which is identical to that shown in Fig. 5 with the addition of via 36. As described
15 earlier, the surface configuration of carrier 50 can vary. For example, the surface
16 configuration could be similar to that shown in Fig. 3 with the addition of via 36 disposed
17 within its center. The benefit to embedding conductive core 38 within insulator 14 and
18 electrically connecting conductive core 38 to metalized ground surface 16 is that a
19 greater surface area is provided for absorbing and dissipating electromagnetic
20 interference and over voltages without an increase in the overall dimensions of carrier
21 50.

22 Figs. 8 and 9 disclose a further alternate embodiment of the present invention
23 in double-sided carrier 60. Carrier 60 is identical to carrier 50, shown in Figs. 6 and 7,
24 except that it is double-sided as the embodiment shown in Fig. 4 with the addition of via

1 36 disposed through the bottom of carrier 60 electrically coupling metallized ground
2 surface 16 along the bottom of carrier 60 to conductive core 38. This embodiment
3 provides a ground having an increased surface area to both surface mount differential
4 and common mode filter components 12a and 12b coupled to the top and bottom of
5 double-sided carrier 60.

6 An additional embodiment of the present invention, connector carrier 100, is
7 illustrated in Fig. 10. In this embodiment the surface mount component carrier is
8 directly incorporated within an electronic connector. Connector carrier 100 is comprised
9 of a metallized plastic base 112 having a plurality of apertures 98 disposed through
10 base 112, each of which receives a connector pin 102. Although not shown, portions
11 of each connector pin 102 extends through base 112 and out of the front 110 of carrier
12 carrier 100. The portions of pins 102 extending from the front 110 of carrier
13 100 form a male connector which is then, in turn, received by a female connector as is
14 known in the art. The same configuration could be implemented on a female connector
15 which then receives male pins. Coupled to both edges of connector carrier 100,
16 although only one edge is shown, is mounting base 114 which elevates base 112 from
17 a surface such as a printed circuit board. The particular embodiment of connector 100
18 shown in Fig. 10 is of a right angle connector in which the tips of pins 102 would be
19 inserted within apertures in a printed circuit board. Pins 102 would then be soldered
20 to the individual apertures or pads in the printed circuit board to provide electrical
21 connection between pins 102 and any circuitry on the printed circuit board. To provide
22 for the coupling of a plurality of differential and common mode filters 104 between the
23 various connector pins 102, two insulating bands 106 and 107 are provided to
24 electrically isolate each of the connector pins 102 from the metallized plastic base 112

- 1 which covers substantially all of the surface area of connector carrier 100.
- 2 Referring to Fig. 11, the relationship between insulating bands 106 and 107, metalized plastic base 112 and differential and common mode filter 104 will be explained in more detail. While only one example is shown, both insulating bands 106 and 107 include a plurality of conductive pads 108 which surround apertures 98. Conductive pads 108 are electrically coupled to connector pins 102 disposed through apertures 98. Insulating bands 106 and 107 provide a non-conductive barrier between the conductive pads 108 and the metalized plastic base 112. Surface mount components, such as differential and common mode filter 104, are positioned between insulated bands 106 and 107 so that first differential conductive band 116 of filter 104 comes in contact with a portion of a conductive pad 108 and second differential conductive band 118 comes in contact with a portion of an opposite conductive pad 108. Insulated outer casing 122 of filter 104 slightly overlaps onto each insulating band 106 and 107 and metalized plastic base 112 to maintain electrical isolation of first and second differential conductive bands 116 and 118 and metalized plastic base 112 of connector carrier 100. Because metalized plastic base 112 runs between insulating bands 106 and 107, common ground conductive bands 120 of filter 104 come in contact with the metalized plastic base 112. As described earlier, each of the various conductive bands of filter 104 are comprised of solder terminations which, when subjected to known solder reflow methods, physically and electrically couple to any metallic surfaces which they come in contact thereby permanently coupling the surface mount components, i.e. filter 104, to connector carrier 100. As in the previous embodiments, connector carrier 100 allows miniature, fragile surface mount components to be used without subjecting those components to increased physical

1 stress which can cause damage to the components, lowering production yields and
2 increasing overall production costs. Metalized plastic base 112 also provides a large
3 conductive surface area connected to the ground terminations of filter 104 improving
4 the ground shield used to absorb and dissipate electromagnetic interference and over
5 voltages.

6 As described herein with relation to each of the differential and common mode
7 filter carrier embodiments, the primary advantages are the additional physical strength
8 the filter carriers provide to the differential and common mode filters and the increased
9 shield and ground effects provided by the enlarged conductive surface areas coupled
10 to the differential and common mode filters.

11 Figs. 12A and 12B show the carrier energy conditioning circuit assembly 400
12 which resulted from the combination of the previously described component carriers
13 with the differential and common mode filter 12. Shown in Fig. 12A, differential and
14 common mode filter 12 is placed upon conductive ground surface 402 making physical
15 contact between conductive ground surface 402 and common ground conductive
16 electrode bands 26. First and second differential conductive bands 30 and 28 are
17 placed upon insulation pads 408 with differential signal conductors 404 and 406
18 disposed through each insulation pad 408. First differential electrode band 28 and first
19 differential signal conductor 404 are then further coupled physically and electrically to
20 each other through a well known means in the art such as solder 410. In addition,
21 second differential electrode band 30 and second differential signal conductor 406 are
22 coupled physically and electrically to one another and common ground conductive
23 electrode bands 26 are coupled physically and electrically to ground area 402.

24 The internal construction of differential and common mode filter 12 electrically

1 isolates differential signal conductor 404 and first differential electrode band 28 from
2 second differential signal conductor 406 and second differential electrode band 30. The
3 internal construction of the differential and common mode filter 12 creates a capacitive
4 element coupled between the first and second differential signal conductors 404 and
5 406 and creates two capacitive elements, one coupled between the first differential
6 signal conductor 404 and the common conductive ground surface 402 and the other
7 coupled between the other second differential signal conductor 406 and the common
8 conductive ground surface 402. While this arrangement of line-to-line and line-to-
9 ground filtering is occurring the first and second differential signal conductors 404 and
10 406 remain electrically isolated from one another. From Fig. 12B it can be seen that
11 first and second differential electrode bands 28 and 30 are prevented from coming into
12 direct physical contact with conductive ground surface 402 due to insulating pads 408
13 interposed between differential signal conductors 404 and 406 and the conductive
14 ground surface 402.

15 The combination of the differential and common mode filter 12 with its capacitive
16 elements coupled line-to-line between differential signal conductors 404 and 406 and
17 line-to-ground between the differential signal conductors 404 and 406 and conductive
18 ground surface 402 provides substantial attenuation and filtering of differential and
19 common mode electrical noise. At the same time the combination also performs
20 simultaneous differential line decoupling. Another benefit provided by the combination
21 include mutual cancellation of magnetic fields generated between differential signal
22 conductors 404 and 406. By connecting the common ground conductive electrode
23 bands 26 to a large conductive ground surface 402, increased shielding of the ground

1 plane is provided to differential and common mode filter 12 which further enhances the
2 desired functional characteristics of differential and common mode filter 12.

3 The combination of the differential and common mode filter 12 with the internal
4 partial Faraday-like shields electrically connected to conductive ground surface 402
5 cause noise and coupling currents from different elements of carrier energy conditioning
6 circuit assembly 400 to be contained at their source or to conductive ground surface
7 402 without affecting differential signal conductors 404 and 406 or other elements of
8 carrier energy conditioning circuit assembly 400 when differential and common mode
9 filter 12 is attached between differential signal conductors 404 and 406. Carrier energy
10 conditioning circuit assembly 400 reduces, and in some cases eliminates, forms of
11 capacitor parasitics and stray capacitance between differential signal conductors 404
12 and 406. Differential and common mode filter 12 provides these benefits due to its
13 internal, partial Faraday-like shields that almost envelope the internal differential
14 electrodes of differential and common mode filter 12 which connect to ground
15 conductive electrode bands 26. These benefits are significantly increased when the
16 partial Faraday-like shields are electrically connected by ground conductive electrode
17 bands 26 to conductive ground surface 402.

18 Figs. 13A - 13D show one application of carrier energy conditioning circuit
19 assembly 400 used in conjunction with a crystal. Referring to Fig. 13B, differential and
20 common mode filter 12 is physically and electrically coupled between first and second
21 differential signal conductors 404 and 406 and to ground conductive surface 402. In
22 this particular application ground conductive surface 402 is comprised of the metal base
23 of the crystal, which in turn is connected to a metal cover 415 shown in Figs. 13C and

1 13D. First and second differential signal conductors 404 and 406 of carrier energy
2 conditioning circuit assembly 400 are electrically isolated from ground conductive
3 surface 402 by insulation pads 408. Common ground conductive electrode bands 26
4 are electrically connected to ground conductive surface 402 using solder 410 or other
5 similar means. A ground conductor pin 414 is also attached or molded monolithically
6 to conductive ground surface 402 by soldering, welding or casting. Ground conductor
7 pin 414 allows for further connection of crystal component application 416 to a system
8 ground (not shown). The internal construction of the differential and common mode
9 filter 12 creates a capacitive element coupled between the first and second differential
10 signal conductors 404 and 406 and creates two capacitive elements, one coupled
11 between the first differential signal conductor 404 and ground conductive surface 402
12 and the other coupled between the other second differential signal conductor 406 and
13 ground conductive surface 402. While this arrangement of line-to-line and line-to-
14 ground filtering is occurring the first and second differential signal conductors 404 and
15 406 remain electrically isolated from one another. From Fig. 13B it can be seen that
16 first and second differential electrode bands 28 and 30 are prevented from coming into
17 direct physical contact with ground conductive surface 402 due to insulating pads 408
18 interposed between differential signal conductors 404 and 406 and the ground
19 conductive surface 402.

20 Figs. 13C and 13D show the final combination of crystal component assembly
21 416 and its metal housing 415 which provides an additional ground shield for the
22 combination. The carrier energy conditioning circuit assembly 400 shown in crystal
23 component assembly 416 simultaneously filters and attenuates common mode and

1 differential mode electrical noise attributed to such circuitry including such noise found
2 between differential electrical line conductors 404 and 406. Crystal component
3 assembly 416 can also substantially reduce and in some cases eliminate or prevent
4 differential current flow, mutual inductive coupling such as cross talk and ground
5 bounce between either differential electrical line conductor 404 and 406 and the
6 common voltage reference located on ground conductive surface 402. The carrier
7 energy conditioning circuit assembly 400 also simultaneously provides mutual
8 cancellation of opposing magnetic fields attributed to and existing between differential
9 electrical line conductors 404 and 406. In addition, carrier energy conditioning circuit
10 assembly 400 complements the inherent, internal ground structure and internal shield
11 structures that nearly envelope or surround each opposing electrode within differential
12 and common mode filter 12 to substantially improve overall noise attenuation on
13 differential signal conductors 404 and 406 that would otherwise affect and degrade the
14 desired performance of crystal component application 416. The essential elements
15 of carrier energy conditioning circuit assembly 400 consist of differential and common
16 mode filter and decoupler 12 as defined herein with a capacitive element coupled
17 between the first and second differential signal conductors 404 and 406 and two
18 capacitive elements, one coupled between the first differential signal conductor 404 and
19 ground conductive surface 402 and the other coupled between the other second
20 differential signal conductor 406 and ground conductive surface 402 while maintaining
21 electrical isolation between the first and second differential signal conductors 404 and
22 406; at least two energized differential electrical line conductors; and a physical and
23 electrical coupling of common ground conductive electrode bands 26 of differential and

1 common mode filter 12 to ground conductive surface 402. The various elements listed
2 that make up carrier energy conditioning circuit assembly 400 are interconnected using
3 solder 410, conductive epoxy 417 or other means well known in the art.

4 The carrier energy conditioning circuit assembly is created when a differential
5 and common mode filter, of the type shown above or of variations incorporated by
6 reference, is used in any application combination of the specific elements that can be
7 assembled on, into or within an energized, electrical circuit system. The addition of the
8 differential and common mode filter to the existing circuit creates a unique electrical
9 circuit system. The electrical circuit system including the differential and common mode
10 filter can be located on or in, but not limited to, a carrier, an interposer, a PCB, a
11 connector, an IC package, a chip carrier, or a silicon die. The electrical circuit system
12 comprises an energy source or load energized through a minimum of one or more
13 phased or oppositely phased or charged line conductor elements to receive
14 conditioning. These can consist of single or mixed elements, such as, but not limited to,
15 traces, vias, wires, conductors, or any other element that can be electrically charged.

16 The invention consists of a differential and common mode filter and decoupler
17 connected internally within an integrated circuit in order to filter and protect the
18 integrated circuit power bus. The invention functions without debilitating ground
19 return EMI or parasitics returning back through the differential and common mode
20 filter and decoupler, which would otherwise affect the integrated circuit. Other
21 advantages are in the elimination of multiple external and/or internal decoupler
22 capacitors that have been needed in the past. The prior art has required decoupling
23 capacitors both on the outside and inside of the integrated circuit package or

1 substrate.

2 The present invention consisting of the differential and common mode filter
3 and decoupler internally connected to the power bus lines of an integrated circuit
4 makes up a single unit that handles and/or conditions all energy sources required by
5 the load demands of an integrated circuit through a single point of conditioning. The
6 invention also provides a reference ground for all power and return lines, traces or
7 conductors entering and leaving the integrated circuit package or substrate.

8 In embodiments of the present invention shown in Figs. 14-20, various
9 differential and common mode filters are used in combination with a carrier substrate
10 of the type used in an integrated circuit package such as, but not limited to, a digital
11 signal processor or microprocessor, to form a carrier energy conditioning circuit
12 assembly. The substrate carrier is typically made of a conventional material such as,
13 but not limited to, glass, ceramic, special thermoplastic, or any conventional material
14 used in the electronics industry. The carrier may have one or more layers in which a
15 power bus, a return bus, and a ground plane are configured. The ground plane is
16 typically made of conventional trace material such as, but not limited to, gold, copper,
17 conductive layering or doping, etc. The ground plane may either be floating or
18 electrically connected to the system ground, chassis ground, etc. The combination of
19 the layered architecture and carrier can dissipate and/or accept energy in a balanced
20 manner from the circuit, acting as a central energy source or reservoir through multiple
21 conductive pathways. When the differential and common mode filter attached to an
22 external conductive area or ground, the external conductive area or ground areas are
23 extended, effectively shielding and enveloping each differential electrode and the

1 effectiveness of the overall conditioning functions are enhanced. The undesirable
2 signals (noise) or transients can dissipate over a broader surface area of the extended
3 conductive area or larger external ground plane. The differential and common mode
4 filter can be attached to the carrier on top, on bottom, or imbedded within the carrier as
5 discussed below.

6 Referring now to Fig. 14A, a top view of an integrated circuit 220 is shown. The
7 center area of integrated circuit package 220 is typically covered with a glob sealant or
8 a substrate cover as is commonly used in the electronics industry, to electrically insulate
9 and protect the integrated circuit components. This top cover has been removed to
10 reveal the interior of integrated circuit package 220, which comprises a novel substrate
11 carrier 180 attached to a silicon die (not shown) of the integrated circuit that is mounted
12 in a lead frame 221. Carrier substrate 180 has a power bus trace 182, a return bus
13 trace 184, and a ground plane 186 all attached in a single layer to a top surface of the
14 carrier 180. Bus traces 182 and 184 are shown in a concentric pattern on the top
15 surface of the carrier 180. The concentricity of the bus traces 182 and 184 provide a
16 cancellation of inductance due to the opposite current flow through the bus traces. Bus
17 traces 182 and 184 are shown in a concentric octagonal pattern. While the present
18 invention is not limited to a particular shape, it is recognized that concentric bus traces
19 having 45 degree traces result in a reduction of noise reflections and ground bounce
20 when compared to concentric traces having 90 degree trace turns, such as in a square
21 or rectangular configuration. In the same manner, concentric circular or elliptical bus
22 traces will result in a greater reduction of noise reflections and ground bounce than
23 concentric traces having 45 degree trace turns.

1 Still referring to Fig. 14A, a plurality of loads 188 are connected to traces 182
2 and 184 by bond wires 190, jumper wires, or other conventional interconnects used in
3 the electronics industry. The bond wire 190 lengths are kept as short as possible to
4 reduce stray impedance. Loads 188 are representative of internal loads of the
5 integrated circuit 220 and comprise the various functions and devices supported by the
6 integrated circuit. Loads 188 are typically connected by bond wires 190 to leads 223,
7 which surround the perimeter of the integrated circuit 220. The loads 188 are symbols
8 which are shown on the top surface of the lead frame for communication convenience.

9 Ground plane 186 comprises three regions; a ground trace 222 that is concentric
10 with and in between bus traces 182 and 184, an outer ground area 224 that surrounds
11 the outermost bus trace 184, and an inner ground area 226 that is surrounded by the
12 innermost bus trace 182. Ground trace 222 separates and provides some inductive
13 cancellation, cross talk suppression, and line to line isolation of the bus traces 182 and
14 184. The conductive surfaces of the bus traces 182, 184 are electrically separated from
15 ground plane 186 by open areas on the surface of substrate carrier 180, which are
16 generally concentric with the bus traces 182, 184.

17 To allow for insertion of a differential and common mode filter 200, each of bus
18 traces 182 and 184 have a predetermined space of physical separation between them.
19 The integrated circuit package is designed such that multiple power entry points are
20 reduced to one pair of power entry pins 82 and 83 which are connected to the traces
21 182, 184 by bond wires 190 or other conventional interconnects. Differential and
22 common mode filter 200 is located in a predetermined position as close as possible to
23 power entry pins 82 and 83 which also corresponds to the predetermined space of

1 physical separation between traces 182 and 184. The single power entry portal
2 represented by pins 82 and 83 and the proximity of the filter 200 to the power entry
3 portal reduces the noise that can enter or exit the integrated circuit and interfere with
4 circuitry both internal or external to the integrated circuit package.

5 Ground areas 222, 224, and 226 are interconnected by a single point ground
6 area 228 (see Fig. 14B) which is located directly beneath the differential and common
7 mode filter 200. The ground layer 186 of the carrier substrate 180 in combination with
8 the positioning of the filter 200 in proximity to the power entry pins 82, 83 results in
9 isolation of noise generated by the integrated circuit package 220 from the external
10 circuitry such as, but not limited to, a printed circuit board.

11 Differential and common mode filter 200 comprises first differential electrode
12 bands 202, second differential electrode bands 206, and common ground conductive
13 bands 204, all separated from each other by insulated outer casing 208. The filter 200
14 is oriented on the carrier 180 such that the first differential electrode bands 202 and the
15 second differential electrode bands 206 can be attached to the ends of the traces 182
16 and 184 to connect the individual traces and complete the circuit path. Continuity of
17 traces 182 and 184 reduces reflections and ESL. Common ground conductive bands
18 204 are electrically connected to the ground plane 186 through single point ground area
19 228 shown in Fig. 14B. The connection of the common ground conductive bands 204
20 and the differential electrode bands 202 and 206 can be accomplished using industry
21 standard means such as solder, springs, etc., as previously discussed herein. The
22 alignment of filter 200 in parallel with the loads and the arrangement of the single layer
23 carrier substrate 180 results in improved decoupling performance.

1 Referring now to Fig. 15, generally the same top view of an integrated circuit 220
2 is shown, except that the orientation of filter 200 is rotated 90 degrees. This rotation
3 requires minor modifications related to the mounting of the filter 200, and the location
4 of differential electrode bands 202 and 206. The differential electrode bands 202 and
5 206 are now on the same longitudinal side of the filter 200, respectively, instead of
6 opposite sides as shown in Fig. 14A. The common ground conductive bands 204 are
7 attached to a single point ground area (not shown) underneath the filter 200 which
8 connects the ground areas 222, 224, and 226 to form ground plane 186 in a similar
9 manner as described for the previous embodiment.

10 Although not shown or depicted in Figs. 14A and 15, it is noted that carriers 180,
11 280 should be at least the size of the integrated circuit 220 it is covering so as not to
12 allow sneak currents to couple back on the floating image reference created by the
13 energized energy conditioning circuit assembly.

14 The power bus 182, return bus 184 and ground plane 186 can be imbedded in
15 the carrier substrate on different levels. Referring now to Fig. 16A, a top plan view of
16 a carrier substrate 280 is shown having a power bus trace 182 and a return bus trace
17 184 attached to a top surface thereof. A ground plane 186 is attached to a bottom
18 surface of the carrier 280 as shown in a front cross-sectional view in Fig. 16B and side
19 cross-sectional view Fig. 16C. A plurality of loads 188 are connected to traces 182 and
20 184 by bond wires 190, or other conventional interconnects used in the electronics
21 industry. The loads 188 are internal microprocessor and/or integrated circuit loads
22 representing the various functions and devices supported by the microprocessor and/or
23 integrated circuits, and are typically connected thereto by bond wires attached to leads,

1 which surround the perimeter of the integrated circuit (not shown). The loads 188 are
2 shown as symbols on the top surface of the carrier for ease of understanding. The
3 traces 182 and 184 are shown in a concentric pattern on the top surface of the carrier
4 280. The concentricity of the traces 182 and 184 provide a cancellation of inductance
5 due to the opposite current flow through the bus traces, as previously discussed.

6 As in the previous embodiment, differential and common mode filter 200 is
7 located in a predetermined position on substrate carrier 280 as close as possible to
8 power entry pins 82 and 83 and at a predetermined space of physical separation
9 between each of the traces 182 and 184. The single power entry portal represented
10 by pins 82 and 83 and the proximity of the filter 200 to the power entry portal reduces
11 the amount of noise that can enter or exit the integrated circuit and interfere with the
12 circuitry, both internal and external to the integrated circuit package.

13 Differential and common mode filter 200 is oriented on the carrier 280 such that
14 the first differential electrode bands 202 and the second differential electrode bands 206
15 can be attached to the ends of the traces 182 and 184 to connect the individual traces
16 and complete the circuit path. The common ground conductive bands 204 are
17 electrically connected to the ground plane 186 by vias 192 as shown in Figs. 16B and
18 16C. Via 192 is a small aperture formed in the surface of carrier 280, which is disposed
19 through the body of carrier 280 to provide an electrical connection to ground plane 186
20 on the bottom surface of carrier 280. Although not shown, via 192 includes thru-hole
21 plating to provide the electrical connection. The connection of the common ground
22 conductive bands 204 and the differential electrode bands 202 and 206 can be
23 accomplished using industry standard means such as solder, springs, etc., as

1 previously discussed above.

2 In another embodiment of the invention shown in Fig. 16D, carrier 280 also
3 includes an insulation layer 194 attached underneath ground plane 186. Insulation
4 layer 194 can be made of any predetermined insulating material, such as that of the
5 carrier 280, or of a non-conductive epoxy. The insulation layer 194 prevents electrical
6 connection to the silicon die when the carrier 280 is assembled onto other components
7 within an integrated circuit package (not shown).

8 In another embodiment of the invention, bus traces 182 and 184 are on different
9 layers of the substrate carrier 380. Referring now to Fig. 17A, a top plan view of carrier
10 substrate 380 is shown having power bus trace 182 attached to a top surface thereof.
11 A return bus trace 184 is shown embedded within the carrier substrate 380 at a second
12 layer, as best shown in Figs. 17B and 17C. A ground plane 186 is shown embedded
13 within the carrier substrate 380 at a third layer below the second layer. An insulation
14 layer 194 is optionally attached to a bottom surface of the carrier 380. Returning now
15 to Fig 17A, a plurality of loads 188 are connected to power bus trace 182 by bond wires
16 190. The loads 188 are also connected by bond wires 190 to vias 196 which provide
17 an electrical connection to the imbedded return bus trace 184 on the second layer as
18 shown in Figs. 17B and 17C. Since the bus traces 182 and 184 are on different layers,
19 the traces are aligned directly over top of each other to provide enhanced cancellation
20 of inductance due to the opposite current flow through the bus traces which are the
21 same size, shape, and length.

22 Referring back to Fig. 17A, filter 200 is attached to the top surface of the carrier
23 380 in the same manner as described in relation to Fig. 16A except that the second

1 differential electrode bands 206 are connected to return bus 184 by vias 196. Although
2 not shown, the vias 196 are offset from the return bus 184. The vias 196 are electrically
3 connected to return bus 184 by electrical extension connectors (not shown) positioned
4 between the return bus 184 and via 196. The offset allows the busses 182 and 184 to
5 directly lie over top of each other on different levels without having the via 196 of the
6 return bus 184 coming straight up through the carrier 380 and into the power bus 182.
7 Additionally, power entry pin 82 is also electrically connected to return bus 184 through
8 a bond wire 190 connected to a via 196 that extends down through the carrier to return
9 bus 184.

10 Referring now to Figs. 17B and 17C, insulation layer 194 is attached on the
11 bottom surface of carrier 380 to prevent electrical connection to the silicon die when the
12 carrier 380 is assembled onto other components within the integrated circuit package
13 (not shown). Fig. 17D shows a cross-sectional view similar to Fig. 17B that also
14 shows potting layer 187 over the top surface of carrier 380.

15 In a further embodiment shown in Fig. 18, filter 200 is embedded on a second
16 layer within the substrate carrier 480. First and second differential electrode bands 202
17 and 206 of filter 200 are connected to power bus 182 on a first layer (on the top surface
18 of the carrier 480) and return bus 184 on a fourth layer, respectively, by vias 196
19 extending through carrier 480. Common ground conductive band 204 of filter 200 is
20 connected to the ground plane layer 186 by vias 192. Loads 188, although not shown,
21 are connected to the power bus 182 by bond wires 190 in the same manner as in
22 previous embodiments. In this embodiment, the ground plane 186 is between the
23 power bus trace 182 and the return bus trace 184. Vias 196 from the filter 200 and the

1 loads 188 must extend through apertures in the ground plane 186 to electrically connect
2 to the return bus trace 184. The vias 196 are electrically insulated from the ground
3 plane 186 by insulating band 208 surrounding the interior surface of the apertures of
4 the ground plane 186. Ground separation obtained by positioning of the ground plane
5 186 between the power bus 182 and the return bus 184 results in improved
6 suppression of cross talk and other parasitic effects. As in previous embodiments, bus
7 traces 182 and 184 are on different layers and are aligned directly over top of each
8 other to provide enhanced cancellation of inductance due to the opposite current flow
9 through the bus traces which are the same size, shape, and length.

10 The differential and common mode filter has been presented in many variations
11 both above and in commonly owned patents and patent applications, previously
12 incorporated herein by reference. A further embodiment of the present invention utilizes
13 a variation of the filter previously discussed. Shielded twisted pair feed through
14 differential and common mode filter 300 is shown in Fig. 19A. The difference between
15 this filter 300 and earlier presented filters is the location of first differential electrode
16 bands 302A, 302B and second differential electrode bands 306A, 306B, which are
17 located diagonally from each other, respectively. Common ground conductive bands
18 304 are separated from first and second differential electrode bands 302 and 306 by
19 insulating material 308 as in the previous filter embodiments. Shielded twisted pair feed
20 through differential and common mode filter 300 comprises a minimum of a first and
21 second differential electrode plate 312 and 316, respectively, and a minimum of three
22 common ground conductive plates 314 as shown in Fig. 19B. The plates 312, 314, and
23 316 are stacked and insulated from each other by material 308 as in the previous filter

1 embodiments.

2 Referring now to Figs. 19C and 19D, which show schematic representations of
3 shielded twisted pair feed through differential and common mode filter 300 and how it
4 is used to eliminate differential noise. Current I is shown flowing in opposing directions
5 through first and second differential electrode bands 302A and 306B, crossing over
6 each other, and flowing out through first and second differential electrode bands 302B
7 and 306A. The crossover point of the current I acts as a line to line capacitor while the
8 common conductive ground plate 314 provides line to ground capacitors on either side
9 of the crossover point.

10 In Fig. 19D, the filter 300 is depicted as coplanar plates 312, 314, and 316, with
11 electrode plates 312, 316, each sandwiched by common ground conductive plates 314
12 in a Faraday cage configuration. The current I is shown flowing in opposite directions
13 through the differential electrode plates. Note that the common ground conductive
14 plates 314 are electrically interconnected, but insulated from the differential electrodes
15 as has been disclosed in filter embodiments previously incorporated by reference
16 herein.

17 Referring now to Figs. 19E and 19F, which show schematic representations of
18 shielded twisted pair feed through differential and common mode filter 300 and how it
19 is used to eliminate common mode noise. Current I is shown flowing in the same
20 directions through first and second differential electrode bands 302A and 306A,
21 crossing over each other, and flowing out through first and second differential electrode
22 bands 302B and 306B. The crossover point of the current I acts as a line to line
23 capacitor while the common conductive ground plate 314 provides line to ground

1 capacitors on either side of the crossover point.
2 In Fig. 19F, the filter 300 is again depicted as coplanar plates 312, 314, and 316,
3 with electrode plates 312, 316, each sandwiched by common ground conductive plates
4 314 in a Faraday cage configuration. The current I is shown flowing in the same
5 direction through the differential electrode plates. Note that the common ground
6 conductive plates 314 are electrically interconnected, but insulated from the differential
7 electrodes as has been disclosed in filter embodiments previously incorporated by
8 reference herein.

9 Referring now to Figs. 20A, 20B, and 20C, the shielded twisted pair feed through
10 differential and common mode filter 300 is shown embedded within an integrated circuit
11 package 320. Fig. 20A shows a top plan view of an integrated circuit package 320 with
12 a top insulating layer 322 removed to reveal power bus trace 324 and return bus trace
13 326 servicing internal loads 188 through bond wires 190 which are connected to leads
14 319 surrounding the perimeter of the integrated circuit package 320. The bus traces
15 324, 326 are shown as concentric squares which provide a cancellation of inductance
16 due to the opposite current flow through the bus traces. Note that the traces 324, 326
17 are connected to vias 196 at the center of the integrated circuit 320 in a manner that the
18 connecting via 196 to each respective trace 324, 326 are positioned diagonally from
19 each other for connection to shielded twisted pair feed through differential and common
20 mode filter 300.

21 Turning now to Fig. 20B, a cross-sectional view shows shielded twisted pair feed
22 through differential and common mode filter 300 embedded within the integrated circuit
23 320 and positioned on ground plane 328 at a second level and connected to the bus

1 traces by vias 196 which extend vertically down from the bus trace level, through
2 ground plane 328 to the bottom surface of the integrated circuit 320. At the ground
3 plane 328 level, the vias 196 are electrically insulated from the ground plane by
4 insulation 330 as best shown in Fig. 20C. As with the previous embodiments, the
5 integrated circuit package is designed such that multiple power entry points are reduced
6 to one pair of power entry pins (not shown). The shielded twisted pair feed through
7 differential and common mode filter 300 is located in a predetermined position as close
8 as possible to the power entry pins which also corresponds to the predetermined space
9 of physical separation between traces 324 and 326, which in this example is shown at
10 the center of the integrated circuit 320, although it is not limited to a particular location.
11 The single power entry portal and the proximity of shielded twisted pair feed through
12 differential and common mode filter 300 to the power entry portal reduces the amount
13 of noise that can enter or exit the integrated circuit 320 and interfere with the remaining
14 circuitry, both internal or external to the integrated circuit package.

15 The ground plane is also shown with vias 332 extending downward from the
16 ground plane 328 to the bottom surface of the integrated circuit 320. The vias 332
17 enable the ground plane 328 to be connected to external ground (not shown) if needed
18 for a particular application. Vias 196 and vias 332 are connected by wire bonds or other
19 conventional interconnects (not shown) to their respective external connections.

20 Another related embodiment is shown in a cross-sectional view in Fig. 21. The
21 main difference between this embodiment and the embodiment shown in Figs. 20A-20C
22 is that shielded twisted pair feed through differential and common mode filter 300 is
23 attached to the bottom of integrated circuit package 320 mounted on a printed circuit

1 board 334. Substrate cover 336 is shown displaced from the integrated circuit 320 to
2 reveal internal loads 188. The bottom of the integrated circuit includes a ground
3 substrate layer 338, which is electrically connected to ground plane 340 on printed
4 circuit board 334 through ball grids 342 or other conventional interconnects and vias
5 344 extending through printed circuit board 334. Common ground conductive bands
6 (not shown) of shielded twisted pair feed through differential and common mode filter
7 300 are attached to ground substrate layer 338 by solder or other conventional means.
8 Bus traces 324, 326 are connected to differential electrode bands (not shown) of
9 shielded twisted pair feed through differential and common mode filter 300 by vias 196.
10 Although not completely shown, both the vias 196 and the differential electrode band
11 attachments are electrically insulated from ground substrate layer 338 by insulation 330.
12 Interconnects 346 and 348 extend downward from vias 196 and are connected to a
13 single power entry portal (not shown) serving the integrated circuit package 320.

14 It should also be evident that using the differential and common mode filters, as
15 compared to the labor intensive aspects of combining discrete components found in the
16 prior art, provides an easy and cost effective method of manufacturing. Because
17 connections only need to be made to either end of electrical conductors to provide a
18 differential mode coupling capacitor and two common mode decoupling capacitors, time
19 and space are saved.

20 As can be seen, many different applications of the differential and common
21 mode filter architecture are possible and review of several features universal to all the
22 embodiments must be noted. First, the material having predetermined electrical
23 properties may be one of a number in any of the embodiments including but not limited

1 to dielectric material, metal oxide varistor material, ferrite material and other more exotic
2 substances such as Mylar film or sintered polycrystalline. No matter which material is
3 used, the combination of common ground plates and electrode plates creates a plurality
4 of capacitors to form a line-to-line differential coupling capacitor between and two line-
5 to-ground decoupling capacitors from a pair of electrical conductors. The material
6 having electrical properties will vary the capacitance values and/or add additional
7 features such as over-voltage and surge protection or increased inductance, resistance,
8 or a combination of all the above.

9 Second, in all embodiments whether shown or not, the number of plates, both
10 common conductive and electrode, can be multiplied to create a number of capacitive
11 elements in parallel which thereby add to create increased capacitance values.

12 Third, additional common ground conductive plates surrounding the combination
13 of a center conductive plate and a plurality of conductive electrodes may be employed
14 to provide an increased inherent ground and surge dissipation area and a Faraday
15 cage-like structure in all embodiments. Additional common ground conductive plates
16 can be employed with any of the embodiments shown and is fully contemplated by
17 Applicant.

18 Fourth, the differential and common mode filter structure has the ability to
19 balance its own electrical characteristics and to effect a cancellation of internal
20 inductance attributed to its structure thus preventing performance disruption of the
21 electrical circuit system line conductors.

22 Fifth, the portability of the differential and common mode filter allows insertion
23 into sub-electrical systems that mate with main electrical circuit system such as, but not

1 limited to, integrated circuit carriers, integrated chip modules, system interposers,
2 connector embodiments or any other sub-electrical systems that are subsequently
3 mated to larger or more sophisticated electrical circuit systems.

4 Finally, from a review of the numerous embodiments it should be apparent that
5 the shape, thickness or size may be varied depending on the electrical characteristics
6 desired or upon the application in which the differential and common mode filter is to
7 be used due to the physical architecture derived from the arrangement of common
8 ground and electrode plates.

9 Although the principles, preferred embodiments and preferred operation of the
10 present invention have been described in detail herein, this is not to be construed as
11 being limited to the particular illustrative forms disclosed. They will thus become
12 apparent to those skilled in the art that various modifications of the preferred
13 embodiments herein can be made without departing from the spirit or scope of the
14 invention as defined by the appended claims.

15

Claims

2 What is claimed is:

1. An energy conditioning circuit assembly for electrical connection between

4 an energy source and a load comprising:

means for conditioning energy propagated from said energy source to said load

6 along at least one conductive pathway; and

means for minimizing the loop area between said energy source and said load.

8 thereby reducing radiation of unwanted energy from said energy conditioning circuit

9 assembly.

19

2. The energy conditioning circuit assembly of claim 1, further comprising

12 means for simultaneously filtering differential and common mode noise propagated

13 along said at least one conductive pathway.

14

3 The energy conditioning circuit assembly of claim 1, further comprising

16 means for decoupling said enemy propagated along said at least one conductive

17 pathway

18

4 The energy conditioning circuit assembly of claim 1, further comprising

29. means for partially suppressing parasitics from said energy conditioning circuit.

21 assembly

23

22

1 5. The energy conditioning circuit assembly of claim 1, further comprising
2 means for protecting said energy source and said load from abnormal energy surges.

3

4 6. The energy conditioning circuit assembly of claim 1, wherein said energy
5 conditioning means is comprised of a layered architecture having at least two
6 differential electrodes and at least three common conductive electrodes, wherein at
7 least one of said common conductive electrodes is positioned between said at least two
8 differential electrodes and at least one of said common conductive electrodes is
9 positioned above and below said at least two differential electrodes in a generally
10 coplanar relationship, wherein each of said common conductive electrodes and said
11 differential electrodes are separated from one another by a dielectric material.

12

13 7. The energy conditioning circuit assembly of claim 1, wherein said loop
14 area minimization means is comprised of a conductive substrate.

15

16 8. An energy conditioning circuit assembly comprising:
17 a conductive substrate coupled to an energized electrical circuit, said electric
18 circuit comprising a source of power and at least one load associated therewith;
19 wherein said conductive substrate comprises at least one layer having
20 conductive ground area, a power conductive path, and a return conductive path; and
21 a layered architecture attached to said conductive substrate comprising
22 at least a first and second differential electrode band and at least one common ground
23 conductive band;

1 wherein said conductive ground area is electrically connected to said at least
2 one common ground conductive band, said power conductive path and said return
3 conductive path are electrically connected between said first and second differential
4 electrode bands, respectively, with said power conductive path and said return
5 conductive path are electrically isolated from one another and from said common
6 ground conductive band; and

7 means for simultaneously receiving and conditioning energy propagating to said
8 load in a differentially balanced manner.

9

10 9. The energy conditioning circuit assembly of claim 8, wherein said ground
11 surface is positioned on a second substrate layer, and wherein said ground surface is
12 connected to said at least one common ground conductive band by at least one via.

13

14 10. The energy conditioning circuit assembly of claim 8, wherein said return
15 conductive path is positioned on a second conductive substrate layer and electrically
16 connected to said second differential electrode bands by a via, and wherein said ground
17 surface is positioned on a third substrate layer and is connected to said at least one
18 common ground conductive band by at least one via.

19

20 11. The energy conditioning circuit assembly of claim 8, wherein said return
21 conductive path and said power conductive path are concentric traces.

22

23 12. An electrical conditioning circuit assembly for an integrated circuit

- 1 comprising:
 - 2 a substrate carrier mounted within said integrated circuit, wherein said substrate
 - 3 carrier comprises at least one substrate layer having a ground plane, a power
 - 4 conductive path and a return conductive path for servicing at least one internal load of
 - 5 said integrated circuit;
 - 6 wherein said power conductive path, said return conductive path, and said
 - 7 ground plane are positioned on said at least one substrate layer such that said power
 - 8 conductive path, said return conductive path, and said ground plane are all electrically
 - 9 isolated from one another; and
 - 10 at least one differential and common mode filter having at least a first and
 - 11 second differential electrode band and at least one common ground conductive band;
 - 12 wherein said at least one common ground conductive band is electrically
 - 13 connected to said ground plane;
 - 14 wherein said first and second differential electrode bands are electrically
 - 15 connected to said power conductive path and said return conductive path with both of
 - 16 said paths electrically isolated from one another and from said common ground
 - 17 conductive band;
 - 18
- 19 13. A substrate carrier for an integrated circuit comprising:
 - 20 at least one substrate layer having a ground plane, a power bus and a return bus
 - 21 for servicing at least one internal load of said integrated circuit;
 - 22 wherein said power bus line, said return bus line, and said ground plane are
 - 23 positioned on said at least one substrate layer such that each is electrically isolated

- 1 from the others; and
- 2 wherein said bus lines and said ground plane each have a predetermined area
- 3 of attachment for electrical connection of a surface mount component.
- 4
- 5 14. An energy conditioning circuit assembly substantially as described herein
- 6 with reference to and as illustrated by the accompanying drawings.

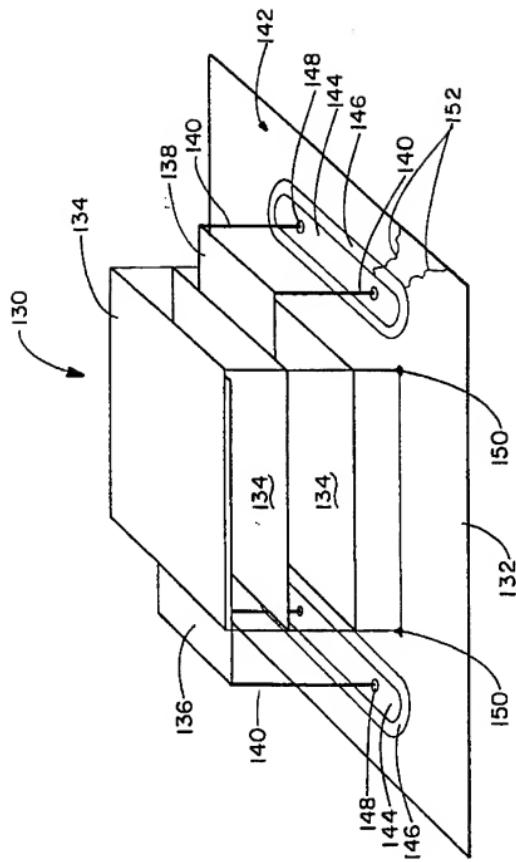


FIG. - 1A

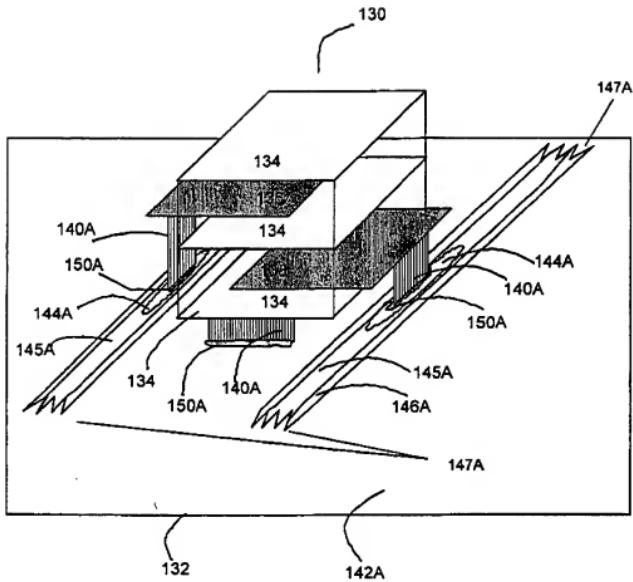
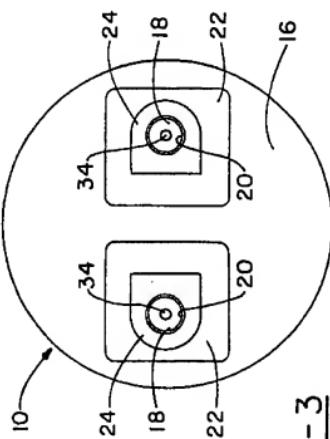
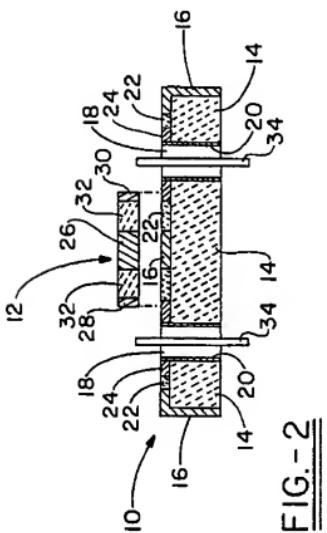
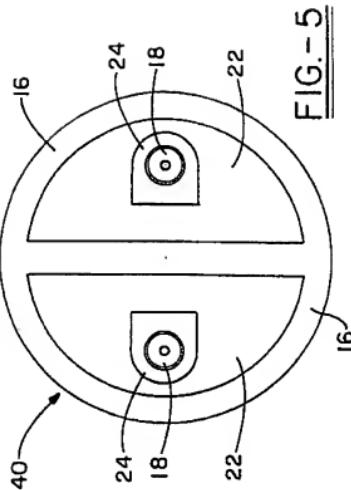
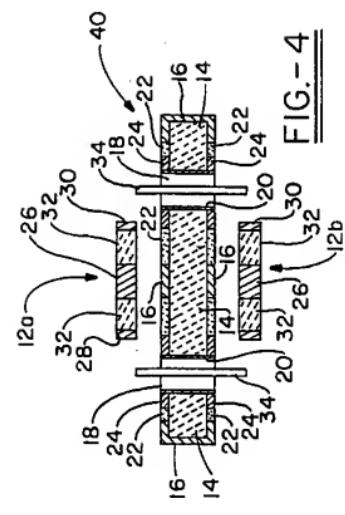
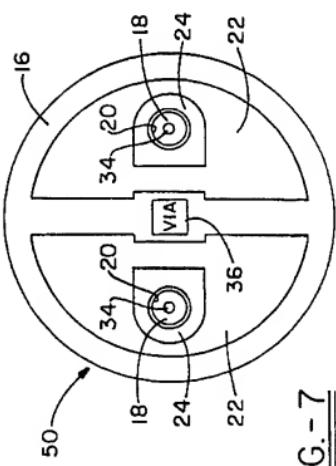
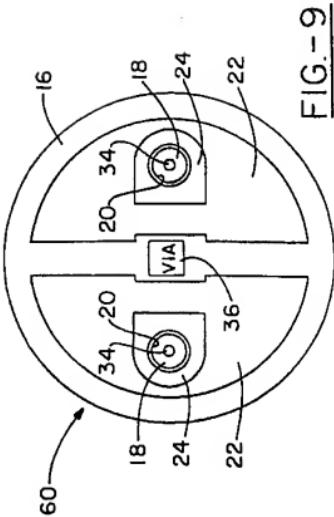
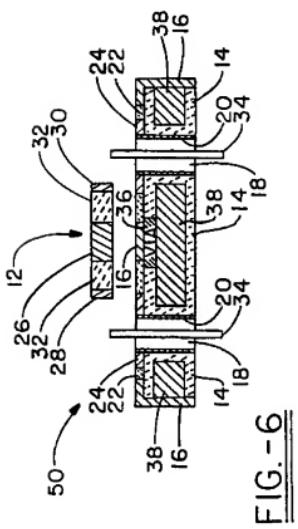
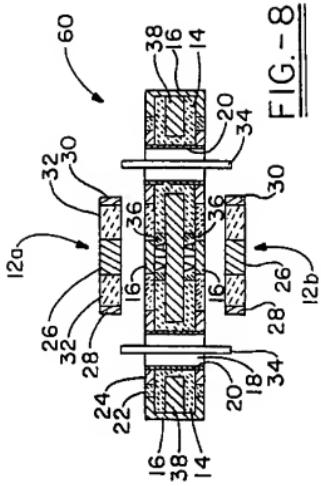
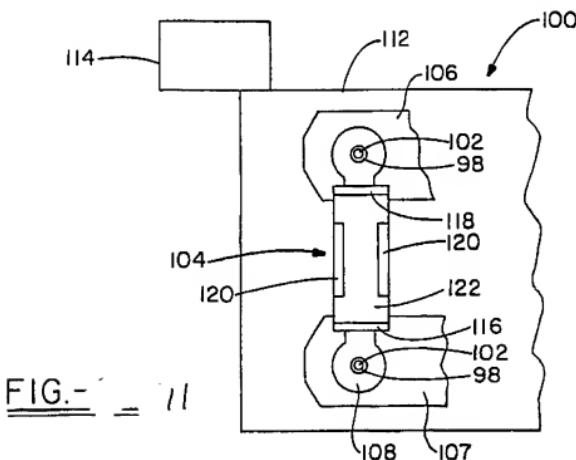
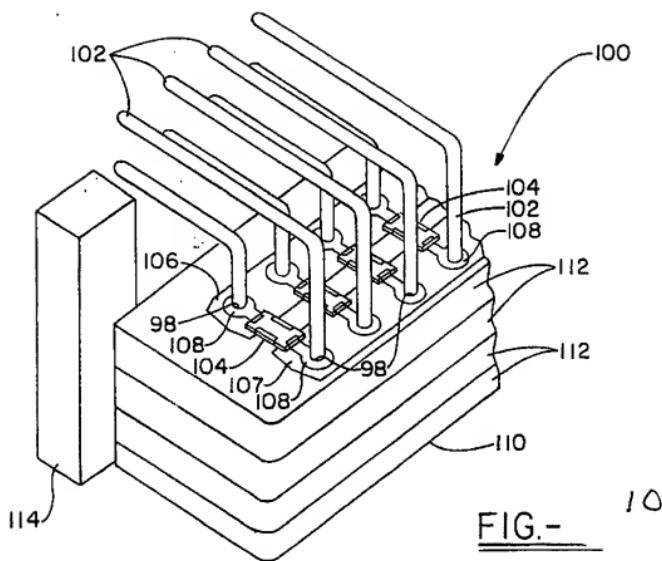


FIG. - 18







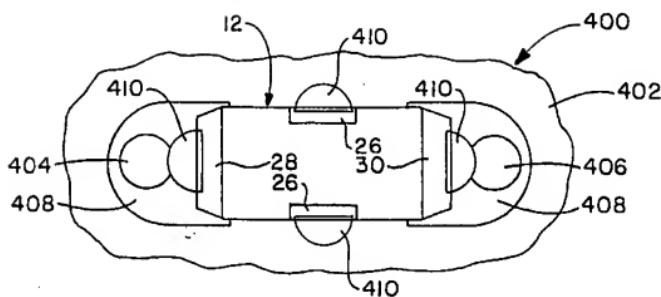


FIG. - 12A

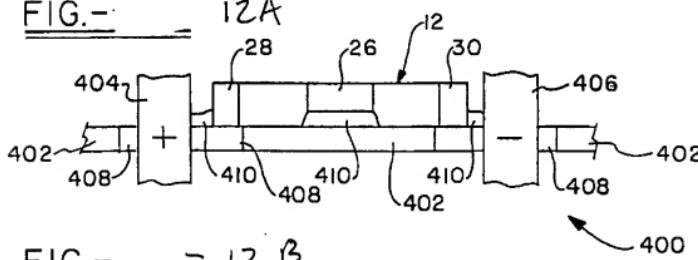


FIG. - 12B

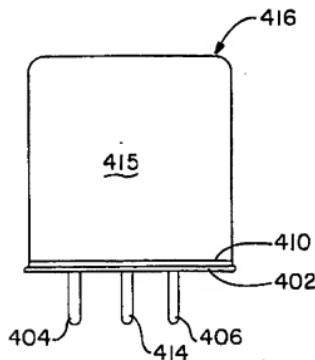


FIG. - 13C

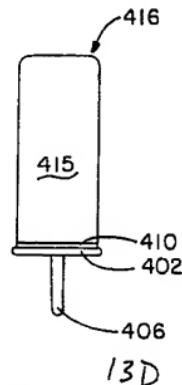


FIG. - 13D

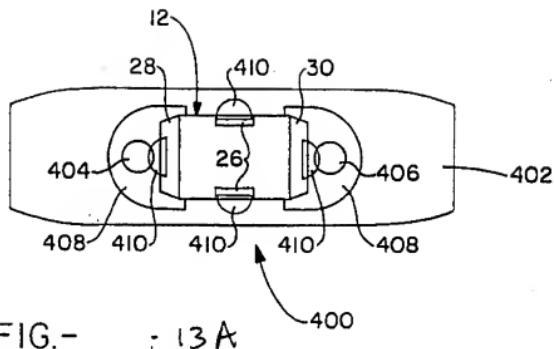


FIG.- : 13A

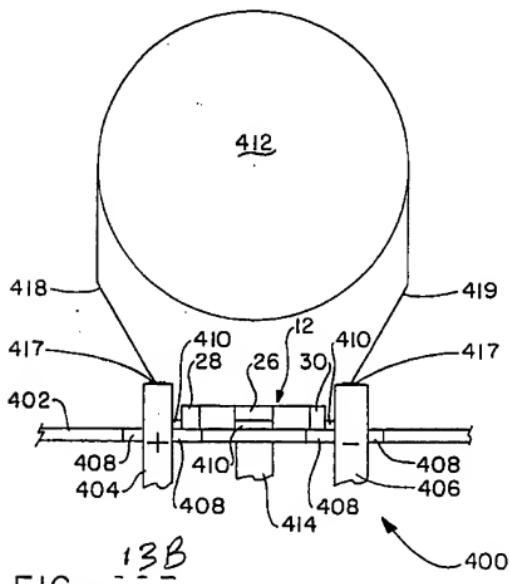


FIG. -- 13B

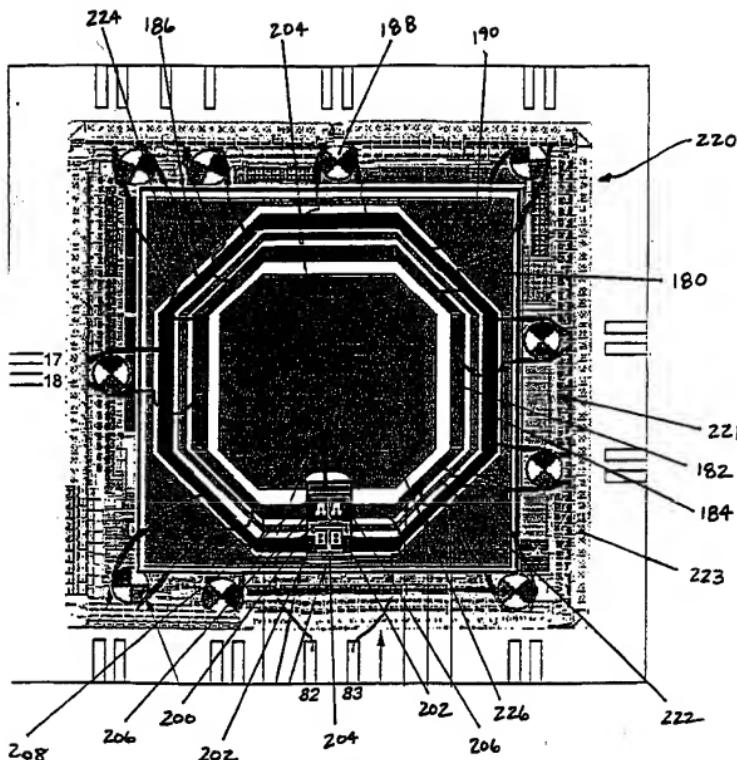


Fig. 14A

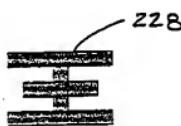


Fig. 14B

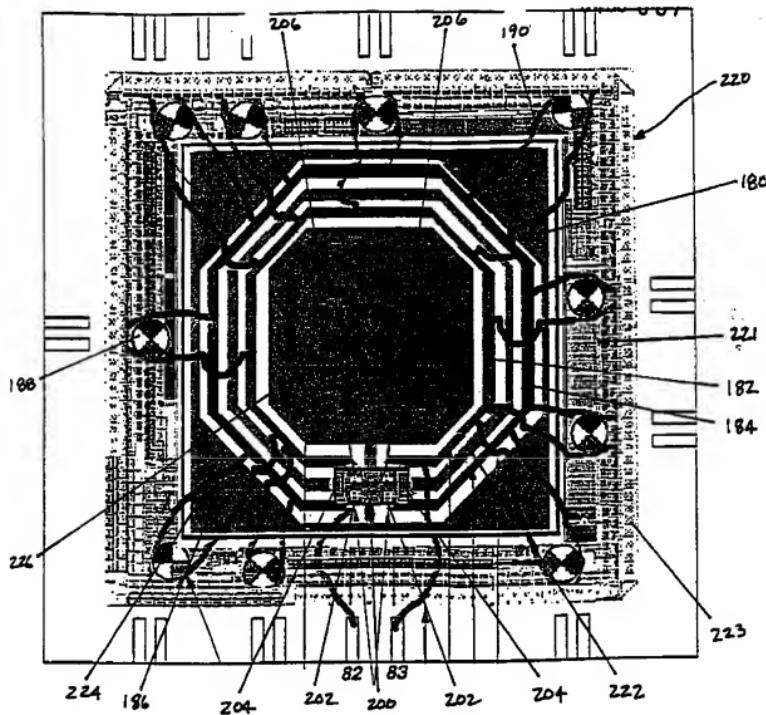


Fig 15

Fig. 16A

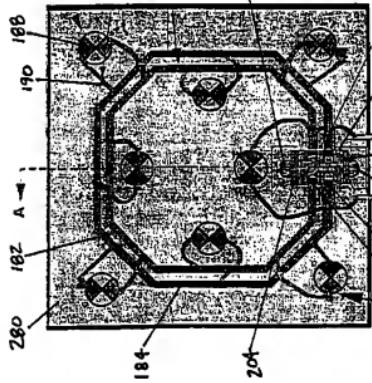


Fig. 16C

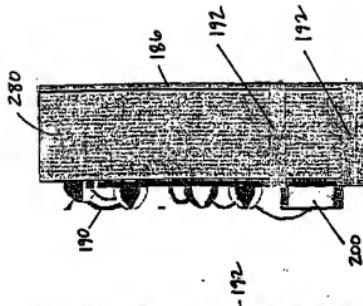


Fig. 16D

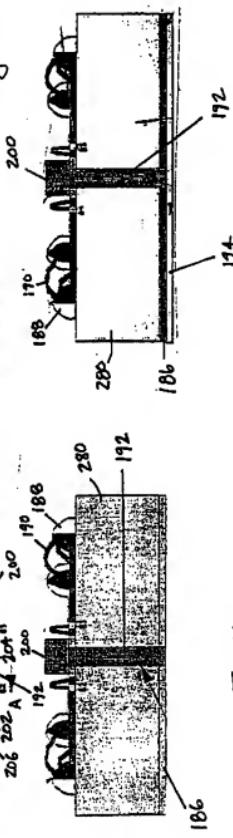


Fig. 16B

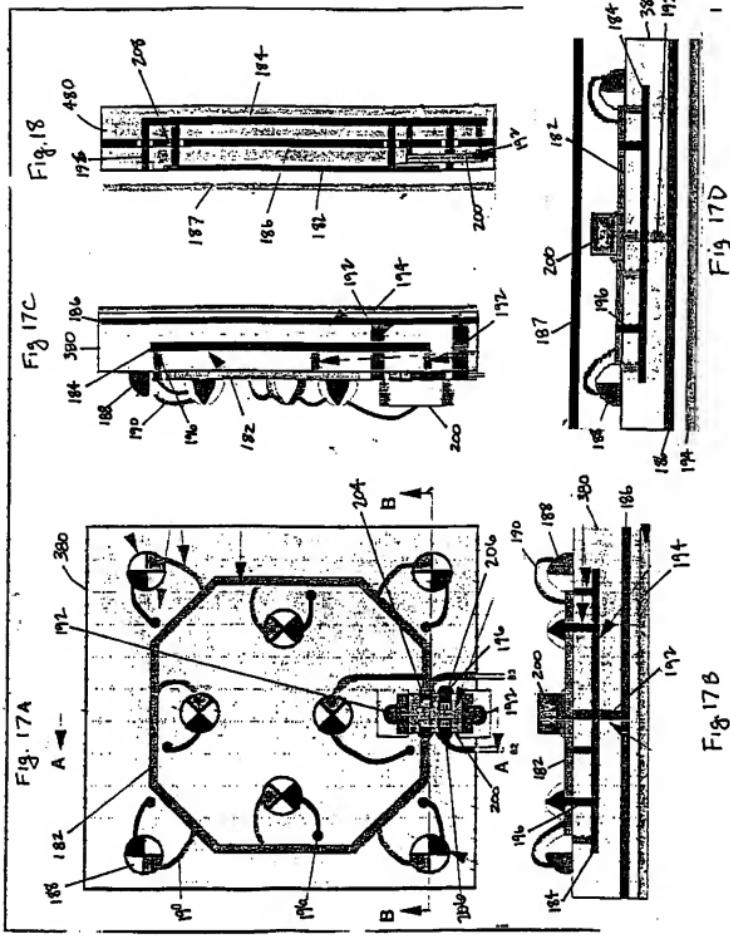


Fig. 19B



Fig. 19A

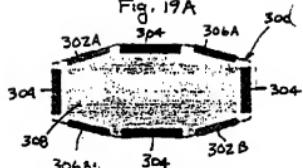


Fig. 19C

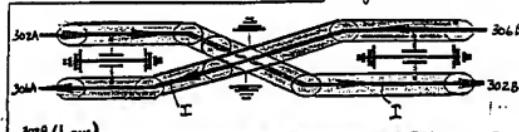


Fig. 19D

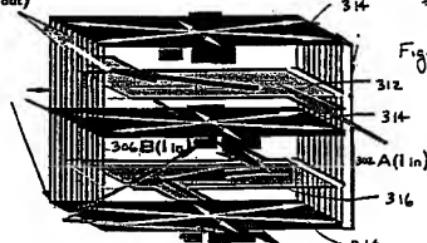


Fig. 19E

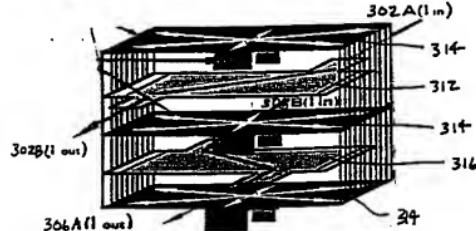


Fig. 19F

Fig. 20A

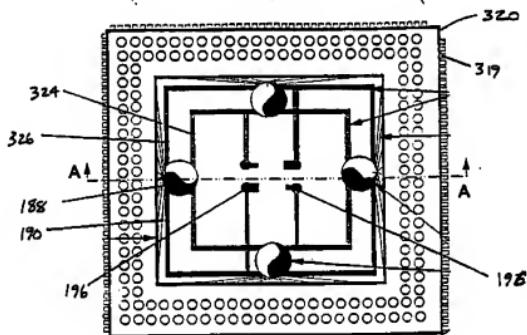


Fig. 20B

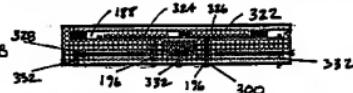
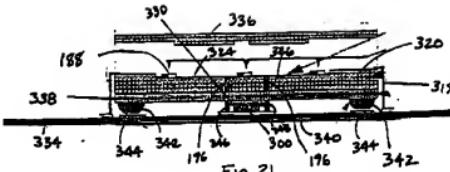
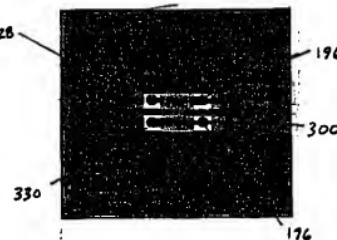


Fig. 20C



INTERNATIONAL SEARCH REPORT

International application No.

PCT/US00/11409

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :H04B 3/00

US CL :333/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 333/181,182, 184; 361/111,113,118

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
EASTElectronic data base consulted during the international search (name of data base and, where practicable, search terms used)
LINE CONDITIONING, DIFFERENTIAL AND COMMON MODE FILTER, ENERGY CONDITIONING

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X,P	US 6,018,448 A (Anthony) 25 January 2000, (25/01/00) col 2 lines 35-67 col.7 and col.8.	1,2, 5-8, 12, 13
A	US 5,142,430 A (Anthony) 25 August 1992 (25/08/92) entire document	2 and 5
A	US 5,337,028 A (White) 09 August 1994 (09/08/94) entire document	2
A	US 5,555,150 A (Newman Jr) 10 September 1996 (10/09/96) entire document	5

Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:	**	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
A document defining the general state of the art which is not considered to be of particular relevance		
B earlier document published on or after the international filing date	***	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
C document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	***	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
D document referring to an oral disclosure, use, exhibition or other means		
E document published prior to the international filing date but later than the priority date claimed	**	document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
23 AUGUST 2000	18 SEP 2000

Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer KIMBERLY E GLENN Telephone No. (703) 305-3942
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